Progress Report on "From Printed Electrolyte-Gated Metal-Oxide Devices to Circuits"

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Printed electrolyte-gated oxide electronics is an emerging electronic technology in the low voltage regime (≤1 V). Whereas in the past mainly dielectrics have been used for gating the transistors, many recent approaches employ the advantages of solution processable, solid polymer electrolytes, or ion gels that provide high gate capacitances produced by a Helmholtz double layer, allowing for low-voltage operation. Herein, with special focus on work performed at KIT recent advances in building electronic circuits based on indium oxide, n-type electrolyte-gated field-effect transistors (EGFETs) are reviewed. When integrated into ring oscillator circuits a digital performance ranging from 250 Hz at 1 V up to 1 kHz is achieved. Sequential circuits such as memory cells are also demonstrated. More complex circuits are feasible but remain challenging also because of the high variability of the printed devices. However, the device inherent variability can be even exploited in security circuits such as physically unclonable functions (PUFs), which output a reliable and unique, device specific, digital response signal. As an overall advantage of the technology all the presented circuits can operate at very low supply voltages (0.6 V), which is crucial for low-power printed electronics applications.

1. Introduction

Printed solution-processed electronic devices open the door for new interesting applications especially where their silicon-based counterparts have limitations as for instance in soft electronics, disposable electronics, large-area applications, or highly customizable electronic circuitry and systems. Therefore, the research area of printed electronics (PE) is growing rapidly since the realization of the first complex circuits in the late 1990s.[1–6] Currently, most of the devices in PE are based on organic materials; state-of-the-art printed field-effect transistors (FETs) consist of lithographically structured or printed electrodes and a printed organic semiconducting channel. As gate-insulators organic, inorganic, or high-*k* dielectrics are very popular in organic FET (OFET) structures. In general, OFETs have field-effect mobility values below 5 $cm^2 V^{-1} s^{-1}$ and most applications based on OFETs require high supply voltages (≥5 V).[1,7–12] Nevertheless, rare examples of low voltage applications based on OFETs can be found in the literature.[13,14]

One approach that is recently gaining interest is to replace the gate dielectric by electrolytes or ion-gels. Herby, the supply voltage requirements of the printed devices can drastically be reduced reaching the sub 1 V operation region. A high specific gate-capacitance value in the range of several tens of μF cm^{-2} is expected for electrolyte-gated field-effect transistors (EGFETs), since a Helmholtz double layer is formed between the gate/electrolyte and the electrolyte/semiconductor interfaces. This high gate-capacitance is responsible for lowering the supply voltage requirements. By applying a potential to the gate-electrode, ions with the opposite sign accumulate at the gate/electrolyte interface. At the same time, the counter ions, inside the electrolyte, accumulate at the electrolyte/semiconductor interface, causing accumulation of charge carriers at the surface of the channel. Both, electronic double layers are known as the Helmholtz double layer. It is also shown that such semiconductors can be ion-impermeable excluding the possibility of electrochemically doping.[15–22] On the other hand, these devices cannot be operated at too high voltages (e.g., >5 V) since high bias stress could lead to chemical reactions and hence device instabilities. Also their maximum speed will be limited by the ionic drift time of

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the electrolytes or ion gels, which are however still compatible with MHz operation frequencies.[15,23,24]

Recent work by Xie et al. includes a D Flip Flop realized in resistor-transistor logic (TR-logic), which is able to operate in the sub 2 V regime. All interconnects and source-, drain-, and gate-electrodes are based on photolithographically patterned gold structures and the channel is based on an organic semiconductor (P3HT). The setup time of the D Flip Flop is less than 50 ms and the operation frequency is only around 5 Hz, however this example shows the potential of EGFETs for the use in complex circuits.[25] A DRAM cell based on the same transistor technology as mentioned before which is able to operate at 1 V supply voltage is also presented in the literature.[26] The retention time of the DRAM cell is greater than 1 min when the write pulse is 20 ms long. The high retention time is related to the fact that EGFETs have a high gate capacitance. With the same EGFET, also a more complex circuit using 23 transistors with the functionality of an H-bridge driver is demonstrated at the supply voltage of 1 V.[11]

In general, the circuit performance is a complex interplay between the DC performance of the in-build devices as well as the parasitic capacitances generated by interconnects as well as the single devices in the particular circuit layout. The choice of the semiconductor channel material is crucial when determining the DC performance of single devices. Owing to their high mobility values, solution processed oxide semiconductors like indium oxide, indium gallium zinc oxide, and zinc oxide have recently become popular as channel material in printed FET technology.[15,27,28] Single crystal oxide semiconductors, for instance, typically show the highest carrier mobility values, in the case of indium oxide specifically in the range of several 100 $cm^2\ V^{-1}\ s^{-1}$.[15,29] Other favorable properties of these wide bandgap oxide semiconductors include stability in air over a wide temperature range, optical transperency, mechanical flexability, and their abilitiy to be easily processable in printing techniques.[15,24,30,31] Promising circuits based on oxide semiconductors have already been successfully measured and show high stability under ambient conditions, lifetimes over several months as well as high performance.[17–20,29,32–34]

The great potential of oxide semiconductors is shown in a ring oscillator based on FETs with indium gallium zinc oxide channel and aluminum oxide dielectric, which oscillates at a frequency of 640 kHz, which translates into a propagation delay of 155 ns per stage. The interconnects and electrodes of the ring oscillator are based on lithographically structured indium tin oxide (ITO) patterns. However, the operating supply voltage is 25 V since a dielectric is used as gate isolator.[35] With the same channel material, a binary coded decimal (BCD) to seven-segement decoder is implemented with an operating frequency of 500 Hz and 5 V supply voltage.[36] Owing to the sensitivity of some oxides to biological components, field-effect-based sensors like electrolyte–insulator–oxide semiconductor structures, oxides were also integrated in sensor applications for detecting pH, penicillin, and DNA.[29,37–39]

2. Electrolyte-Gated Field-Effect Transistors Based on Indium Oxide Channel

In this section, the basic device properties of EGFETs based on indium oxide semiconductor channel material gated with a composite solid polymer electrolyte (CSPE), which combines the benefits of having high performance devices, good printability and, when gated with an electrolyte or ion gel also operation at low supply voltages, are described. The later discussed circuit

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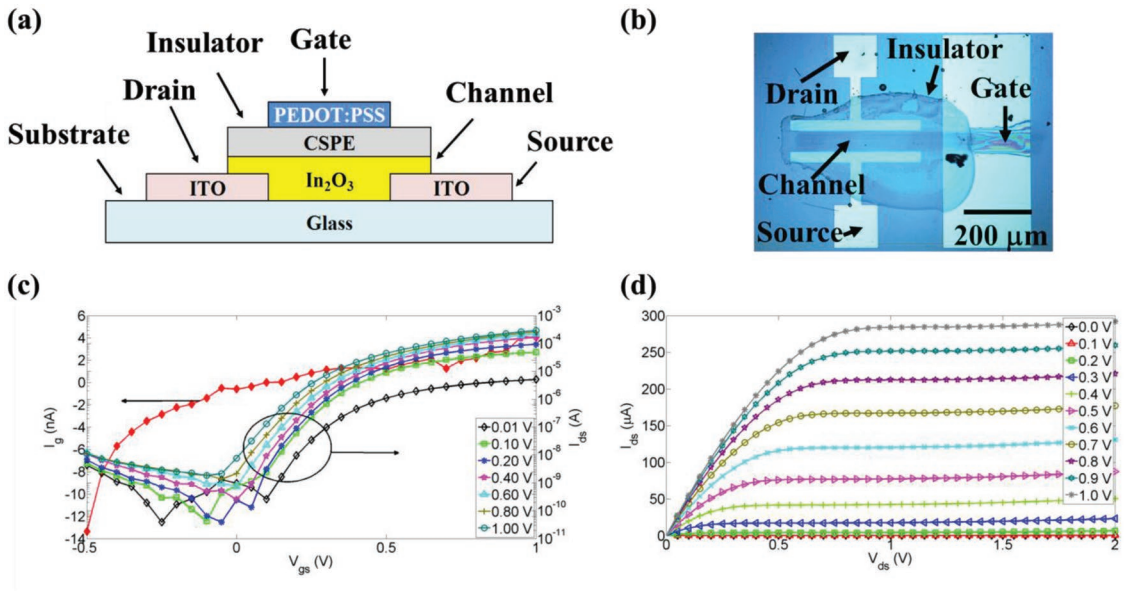

Figure 1. a) Cross section of an EGFET. b) Optical image view of the EGFET. c) Transfer curve: the gate (I_g) and the drain–source (I_{ds}) currents are plotted against the gate–source voltage (V_{gs}) at different drain–source voltages (V_{ds}) (denoted in the legend). d) Output curve: drain–source current (I_{ds}) versus the drain–source voltage at different gate–source voltages (V_{gs}) (please see the legend).

properties can be deduced on the basis of the transistor properties. In **Figure 1**, the cross-sectional view of such an EGFET is displayed, where the channel width (W)/channel length (L) ratio is chosen to be 600 µm/60 µm. In the past, it has been shown that these EGFETs perform reliably over a wide temperature range.[40] The EGFETs were also successfully modeled and integrated into a process design kit (PDK), which supports the circuit design flow.[16,41–43] To achieve high performance EGFETs, the indium oxide films need to be annealed at temperatures around 400 °C.[44] By using chemical or photonic curing methods, the indium oxide film can be cured also at room temperatures.[45–47] Indeed, EGFETs processed at room temperatures show lower field-effect mobility values compared to EGFETs with thermally annealed indium oxide channel. However, fabrication at room temperatures enables the possibility of printing microelectronic circuits onto flexible substrates like plastic or paper. Nevertheless, the contact quality between the indium oxide and the ITO-contacts as well as the interface between the CSPE and the indium oxide needs to be taken into account to improve the field-effect mobility on device level and control the threshold voltage, which is crucial for reliable circuit design. The electrical characteristics of a typical EGFET shown in Figure 1b are presented as follows. Exemplary transfer and output curves of an EGFET are plotted in Figure 1c,d, respectively. The threshold voltage (V_t) and the on/off-ratio of the EGFET are 190 mV and 1.59×10^5, respectively. The subthreshold slope (SS) is 84.8 mV dec^{-1}. The field-effect mobility (μ_{eff}) in saturation at a gate-source voltage (V_{gs}) of 1 V is calculated by using the relation[48]

$$I_{ds} = \frac{W}{L}\frac{\mu_{eff} C_g}{2}\left(V_{gs} - V_t\right)^2 \quad (1)$$

where C_g is the gate capacitance, I_{ds} is the drain–source current, and V_{gs} is the gate–source voltage.[48] The gate capacitance is measured with electrochemical impedance spectroscopy (EIS) and by shortening the drain- and source-electrodes while sweeping the gate potential. Extracted from a parallel plate capacitor test structure, the double-layer capacitance is measured to be ≈4 µF cm^{-2}.[15] However, transferring this measurement and extraction technique to characterize the presented EGFET mentioned above leads to overestimated gate-capacitance of 60 µF cm^{-2} and according to Equation (1) an underestimated field-effect mobility of 0.73 cm^2 V^{-1} s^{-1} at a saturation current of 283 µA and a gate–source voltage of 1 V.

Measuring and extracting the accurate value of the gate capacitance as well as the concluded mobility are a challenge in electrolyte gated devices, since many surface effects between the semiconductor and electrolyte interface, chemical reactions, parasitic and stray capacitances as well as the effective device geometries all interfere and determine the capacitance in the final measurement. Ongoing works employing EIS and cyclic voltammetry on carefully designed test structures together with suitable modeling approaches will hopefully shine some light on this phenomenon in the future.

3. Circuits Based on EGFETs

Indium oxide EGFETs were successfully integrated into several benchmark circuits in the past. The big advantage of these printed circuits is that they are already able to reliably operate at supply voltages far below 1 V.[17–20] This voltage requirement is much lower compared to the state of the art printed applications.[1] In the following, the electrical characteristics of inverters, ring oscillators, latches, and security circuits such as physically unclonable functions (PUFs) based on EGFETs are reported. The presented circuits are designed in TR-logic and all active materials are inkjet-printed. However, the passive structures (interconnects, source and drain

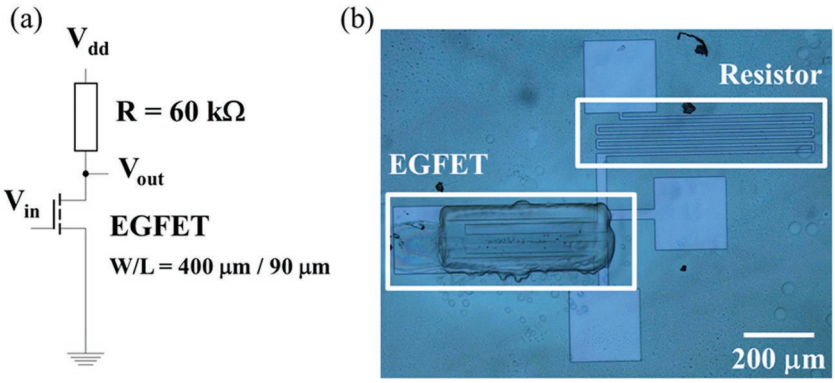

Figure 2. a) Schematic and b) optical image of an inverter based on a resistor and EGFET.

electrodes) are fabricated with e-beam lithography on sputtered ITO on glass but kept within printable dimensions (line thickness is 40 µm).

3.1. Inverter

Inverters are the most basic logic cells in microelectronics. The inverter consists of two elements, one to pull-up and the other to pull-down the output signal. Therefore, if "logic 0" (corresponding to the source voltage level) is applied to the input of the inverter, the output signal is pulled up to "logic 1" (corresponding to the supply voltage level) and vice versa. In conventional CMOS technology, the pull-up network is realized by a p-type FET and the pull-down network by an n-type FET.[49]

Equally performable p-type FETs are rare in oxide electronics, especially when electrolyte gated, which is the reason for the use of a resistor instead of a p-type FET in the pull-up network.[17,19,20] **Figure 2** shows the schematic and an optical image of an inverter with a resistor of 60 kΩ and an EGFET with a W/L ratio of 400 µm / 90 µm. The main difference between the CMOS and TR logic is that static power dissipation is much higher in the TR-logic, since a conductive path between the pull-up and pull-down is always existent. On the contrary in CMOS circuits, a conductive path between the pull up and pull down network is only available during the switching from low to high signals or vice versa. Also the gain of CMOS-based logic devices is higher compared to TR logic designs. The reason for that is that in TR-logic the pull-down FET is not able to compensate the high leakage currents.

At a supply voltage of 1 V, the DC characteristics (transfer curves) show that the output signal of the inverter based on TR-logic alternates with respect to the input voltage between 0.1 and 0.95 V and the maximum gain is ≈4 (**Figure 3**a). However, when the level of the input signal changes it takes some time until a response is measured at the output of the inverter, since the Helmholtz double layer of the EGFET needs to be established or destroyed. The time it takes for the signal to propagate from the input to the output is known as the propagation delay time (t_p) and is measured as the time difference between the input and output signals at 50% signal swing. The rise (t_r) and fall times (t_f) are time differences between 10% and 90% swing of the rising and falling edge of the output signal, respectively.[49] All the aforementioned times are extracted from the transient analysis, where a 1 Hz rectangular signal is applied as the input signal at 1 V supply voltage (Figure 3b). The propagation delay time of the presented inverter is 19.7 ms, the rise and fall times are 8.6 and 64.4 ms, respectively. The large asymmetry between the rise and fall times is related to the fact that establishing a Helmholtz layer is much faster than destroying it. Also the use of a resistor in the pull-up network contributes to this asymmetry since the signal can be pulled up very fast but can only be pulled down very slowly, because the EGFET needs to be switched on in order to pull down the signal.

3.2. Ring Oscillator

Ring oscillator structures are considered to be the key technology characterization components in microelectronics. The ring oscillator can be characterized with a procedure well known from the literature.[17,50,51]

The oscillation frequency of the ring oscillator is twice the sum of the propagation delay (τ_p) time of each inverter stages.

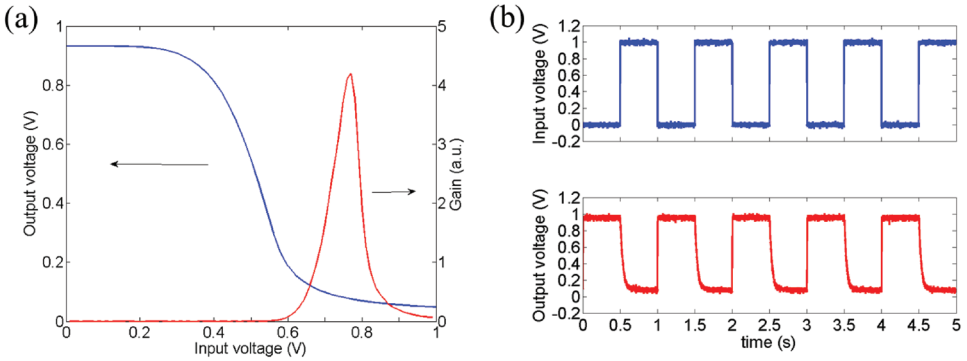

Figure 3. a) DC characteristics and b) transient analysis of an inverter. Both curves are measured at a supply voltage of 1.0 V.

$$f = \frac{1}{2(2\alpha+1)\tau_p} \tag{2}$$

where $2\alpha + 1$ is the number of inverter stages and α a constant. The propagation delay time can be modeled with an RC-network at the output of each inverter stage. Before estimating the switching capacitance (C_{sw}) and switching resistor (R_{sw}) values, required for the RC-network, the current flow during switching (I_{sw}) needs to be quantified, based on the following equation

$$I_{sw} = I_{dda} - I_{ddq}\frac{2\alpha}{2\alpha+1} \tag{3}$$

where I_{dda} is the active and I_{ddq} is the quiescence currents when the oscillation of the ring oscillator is turned on and off, respectively. With the help of the switching current the switching capacitance is calculated as

$$C_{sw} = 2\tau_p \frac{I_{sw}}{V_{dd}} \tag{4}$$

where V_{dd} is the supply voltage of the ring oscillator. The switching resistor can be calculated with the following equation

$$R_{sw} = \frac{V_{dd}}{2I_{sw}} \tag{5}$$

The static power dissipation of the ring oscillator can be estimated by the product of the quiescence current and the supply voltage ($P_{stat} = I_{ddq}\, V_{dd}$). In contrast, the dynamic power consumption contains contributions from the switching current and the supply voltage ($P_{dyn} = I_{sw}\, V_{dd}$). The total power consumption is the sum of the static and dynamic powers.

Figure 4 shows the analyzed ring oscillators. The resistance values of all resistors are set to 60 kΩ and the W/L ratios of all EGFETs are 400 µm/40 µm. However, as can be seen from Figure 4, the first stage of the ring oscillator is a NAND-gate instead of an inverter. The NAND-gate is used to turn on and off the oscillation; if the input signal (V_{enable}) is set to "logic 1" the oscillation is turned on otherwise is turned off. In addition, an inverter is connected to the output of the ring oscillator to avoid inducing noise from the measurements. The power supply of the ring oscillator (V_{ddr} and V_{ssr}) is also electrically isolated from the power supply of the output inverter (V_{ddi} and V_{ssi}) to be able to measure the current flow of the ring oscillator.[17]

The characteristics of the ring oscillator can be seen in **Figure 5**. At a supply voltage of 2 V, the ring oscillator oscillates at a frequency of 352 Hz (Figure 5a). The minimum supply voltage at which the ring oscillator can operate is 0.6 V with a frequency of 256 Hz as shown in Figure 5b. In general, the frequency rises as expected with the applied supply voltage (Figure 5b). The active and quiescence currents increase linearly with the supply voltage since resistors are used in the pull-up network (Figure 5c). The main drawback of the transistor–resistor logic (TR-logic) is the significant static power dissipation, which is in the same range as the active power. The total power consumption at 2 V supply voltage is 138 µW (Figure 5d). While the switching-resistance decreases for supply voltages lower than 0.8 V, the switching capacitance rises in the same voltage levels. For supply voltages larger than 1 V, the switching-resistance starts to saturate at a value ≈26 kΩ and the switching-capacitance saturates at a value of ≈17 nF (Figure 5e,f).[17]

By reducing the channel width of the EGFETs to 200 µm, the same ring oscillators as described above can even operate in the 1 kHz regime. The smaller channel width reduces the parasitic capacitances of the ring oscillator, since overlap between the electrolyte and the passive structure is reduced. However, the other transistor parameters like threshold voltage or field-effect mobility remain in the same range such that the DC performance is not sacrificed.[18]

3.3. SR-Latch

Latches are fundamental digital elements, which enable sequential operations in electronic circuits. They are the building blocks for more complex memory circuits such as Flip Flops and registers. In this regard, we presented an EGFET-based Set–Reset (SR) latch realized by two cross-coupled NOR gates (**Figure 6**).[19]

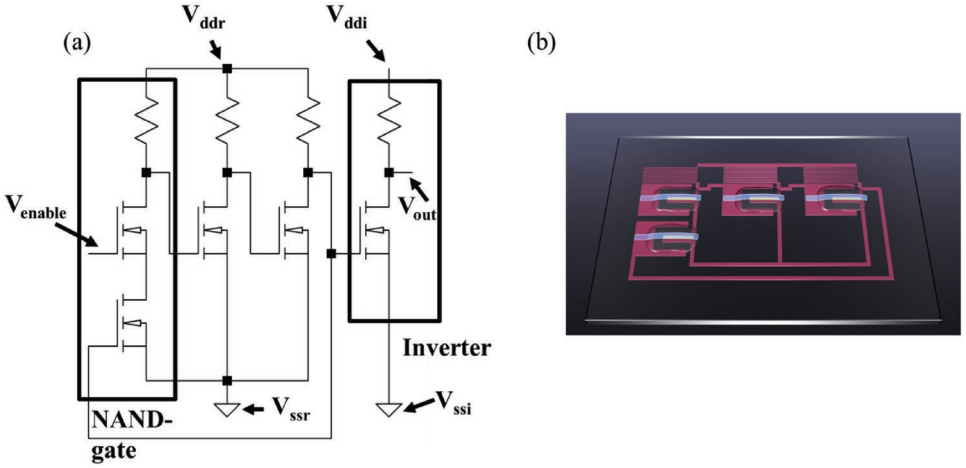

Figure 4. a) Schematic and b) graphical representation of a three-stage ring oscillator.

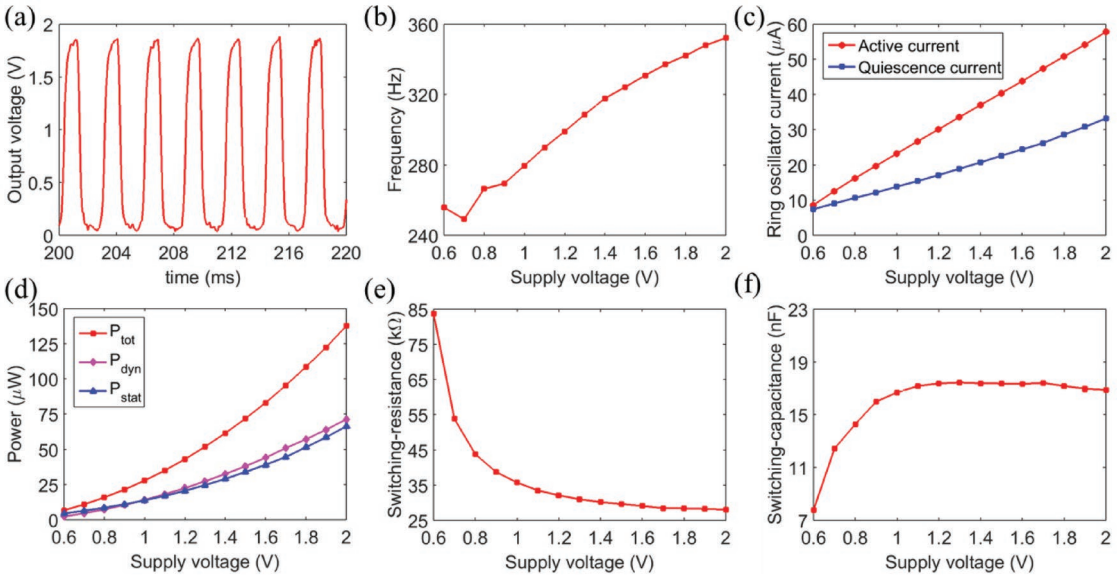

Figure 5. Performance of a three-stage ring oscillator. a) Output voltage (V_{out}) versus the time at a supply voltage (V_{dd}) of 2.0 V and a frequency of 352 Hz. b) Frequency, c) current flow, d) power consumption, e) switching-resistance (R_{sw}) and f) switching-capacitance (C_{sw}) of the three-stage ring oscillator in dependence of the supply voltage (V_{dd}). The measurements are replotted from data in the work presented in ref. [17].

The SR-latch is a level sensitive storage element, which is capable of storing one bit of information. The information stored can be read from the differential output pins (Q, $\bar{Q}$), where a high voltage level is associated to 1, and a low voltage level is related to 0. The outputs are in a constant state when low voltage is applied to both inputs S (Set) and R(Reset). By applying the high voltage level to either of the inputs, the output voltage, and consequently the information stored, is changed. This typical behavior is also illustrated in (**Figure 7**a).

As mentioned earlier due to the scarcity of PMOS transistors in metal oxide technology, the pull-up network consists of two pull-up resistances (TR logic). Nevertheless, a delay of only about 4 ms is achieved for a supply voltage of 1 V with a power of only 5 µW. In general, the power versus supply voltage increases linearly, while the delay decreases quadratically with supply voltage (Figure 7b). The EGFET-channel used in the design has a W/L ratio of 575 µm/40 µm with pull-up resistances of 60 kΩ. The resulting area requirement is 7 mm^2. The measurement was repeated for a period of 12 weeks and no significant performance/power degradation was observed.[19]

3.4. Physically Unclonable Function

Another interesting application for printed electronics are security circuits, that rely on the intrinsic variations inherent to the printed devices caused by the ink dispersions, the ink substrate interaction, the individual printing process, droplet formation and others. As an example very recent work studies so called physically unclonable functions (PUFs) that are used to generate unpredictable secret keys, which are required for secure data transfer, communication and authentication. The feature of unpredictability is the result of uncontrolled process variations of the used devices. The process variation while the device is printed has a direct impact on material properties of the EGFETs and causes a variation in the device electrical parameters such as the threshold voltage, the field-effect mobility as well as the device dimensions. Hence even similarly processed EGFETs with the same channel geometry display different drain–source currents. The measurements of our EGFET devices show that the threshold voltage can vary absolutely in the range of 40–60 mV while the saturated

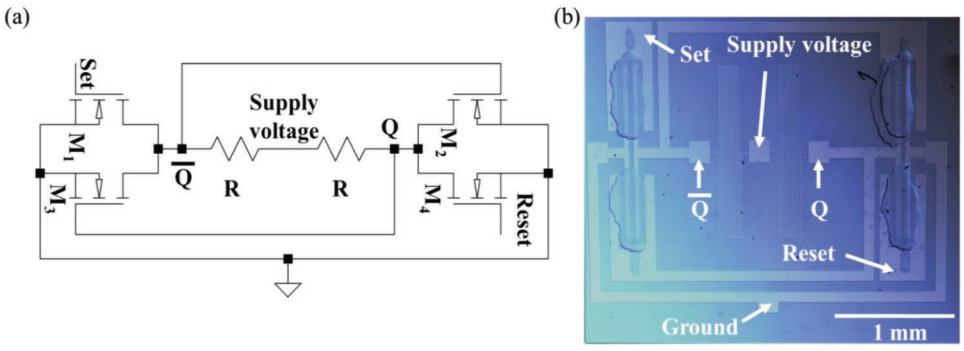

Figure 6. a) Schematic and b) optical image of a latch consisting of resistors and EGFETs.

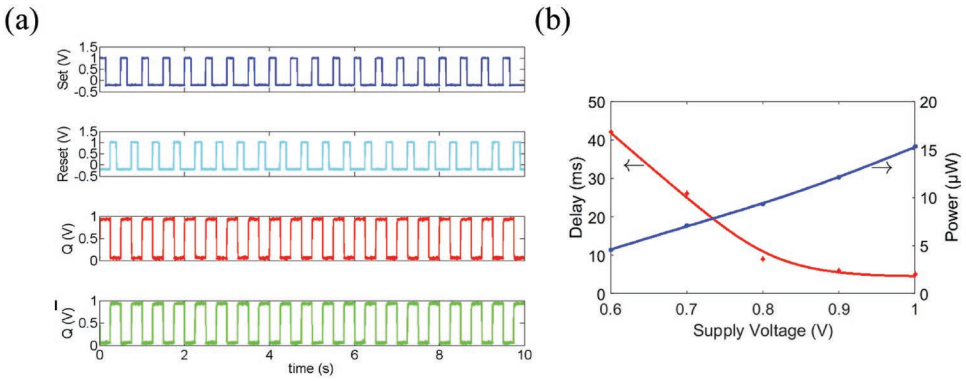

Figure 7. a) Transient characteristics of the latch at a supply voltage (V_{dd}) of 1.0 V. b) Delay/power characteristics of the latch for different supply voltages levels.

drain current is varying between 150 and 300 μA for our chosen PUF transistor geometries. The electrical parameters of an EGFET, can be modeled through a Gaussian mixture model and are described in a variability model published earlier.[43] This variability model is also included in our Process Design Kit and taken into account while designing the PUF. However, the functioning of the PUF circuit is not affected by the variations in threshold voltage and saturation current, because finally one of the two transistors will dominate over the other pulling the signal to the corresponding voltage level. Instead the security metrics such as uniqueness and reliability profit from large intrinsic variations.[52] Also theoretical studies using Monte Carlo (MC) simulations support this argument.[43]

The input signal of the PUF is referred to as the challenge, and causes a device specific response based on the inherent transistor process variations as an output. Hence, each PUF fabricated in the same manner, responds with a unique, nonpredictable output response. Various PUFs core circuits based on inverters or ring oscillators are presented in the literature.[32,52–54]

We have shown a printed PUF based on a memory circuit for identification/authentication applications. The memory like circuit consists of a cross coupled inverter structure and an enable transistor to activate and deactivate the PUF (**Figure 8**a). The resistances of the inverters are chosen to be 40 kΩ and the W/L ratio of the pull-down EGFETs is 200 μm/40 μm. The enable EGFET has a W/L ratio of 400 μm/40 μm.[20]

When the circuit is deactivated (V_{enable} is set to "logic 0") both outputs ($V_{out,1}$ and $V_{out,2}$) are at the "logic 1" level. As soon as the circuit is activated (V_{enable} is set to "logic 1"), one of the outputs $V_{out,1}$ or $V_{out,2}$ stays at the "logic 1" level, while the other is pulled down to the "logic 0" level. The relative drive strength of the EGFET connected to the respective output determines which output is at the "logic 0" or at the "logic 1" level, after turning on the circuit. Due to process variation, one of the EGFETs has a lower threshold voltage (V_t) and higher current than the other; and therefore the stronger EGFET is able to pull down the output to the "logic 0" level while the other output remains at the "logic 1" level. From Figure 8b, it can be seen that the EGFET on the right side is stronger and therefore the output $V_{out,2}$ is pulled down to the "logic 0" level. Also for the presented PUF it is possible to reduce the required supply voltages to values around 0.6 V, which is very interesting for secure data transfer in the Internet of Things (IoT) application domain.[20] A proper understanding and modeling approach for variations in printed electronic devices is needed since it would allow to predict security metrics such as uniqueness and reliability also by simulations in the future.

4. Conclusions

In the past years, printed single devices such as field-effect transistors have proven to be capable to be integrated into printed circuits, although, strictly speaking, most works still include

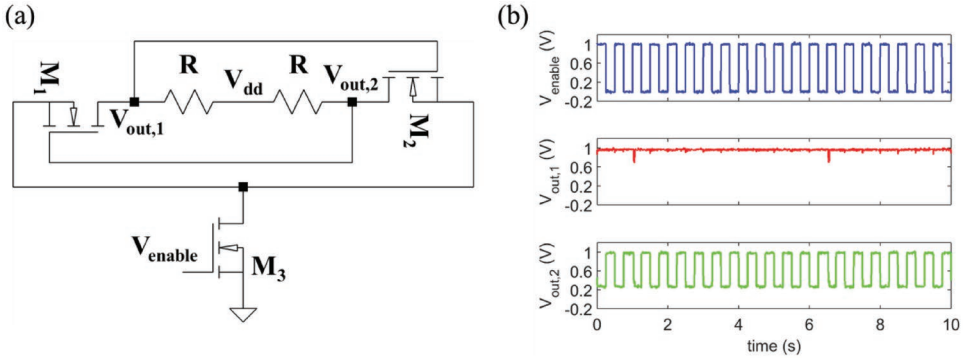

Figure 8. a) Schematic of an EGFET-based PUF in TR logic. b) Measurement of a PUF at a supply voltage of V_{dd} = 1.0 V.

lithographically structured interconnects or electrodes. In the present report focused on work performed at KIT, electrolyte-gated field-effect transistors (EGFETs) with an n-type indium oxide channel material are integrated into circuits by lithographically structured ITO interconnects, source, and drain electrodes sputtered on glass substrates and are well within the feature size typical for printing processes. Circuits discussed in this report include ring oscillators with a digital performance in the range of 350 Hz up to 1 kHz, memory elements in form of an SR-latch as well as security primitives such as physical unclonable functions which rely on the intrinsic device variations to generate a unique and reliable digital output response. Due to the high mobility of the n-type channel and the high gate capacitance developed via the Helmholtz double layer in the described devices all circuits shown here provide ultralow voltage operation down to 0.6 V giving rise to novel low power applications in fields like security, IoT, smart sensors, and wearables. Hence the EGFET technology in combination with appropriate circuit design methodologies could pave the way for high performance and low voltage applications in printed electronics. A challenge to be addressed in the future which is not discussed in this report are printable or solution processable interconnects that are able to form high quality, ohmic contacts with the semiconductor channel material. Furthermore, electrolyte-gating introduces high parasitic capacitances, since it is challenging to print the electrolyte just on top of the channel. The electrolyte drop spreads during printing over the passive structures and forms in accordance with the applied bias a Helmholtz double layer with the passive structures. To enhance the performance of EGFET-based circuits, it will be essential for future work to reduce the unwanted electrolyte area to a minimum. Experiments also showed that the electrolyte is reactive with silver, which can become an issue for highly integrated electronics, especially when the passive structures are printed with commercial silver inks. Future work should include new electrolytes that are silver compatible and some of very recent developments suggest their feasibility and reliability.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

electrolyte gating, memory circuits, oxide electronics, printed electronics, ring oscillators

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